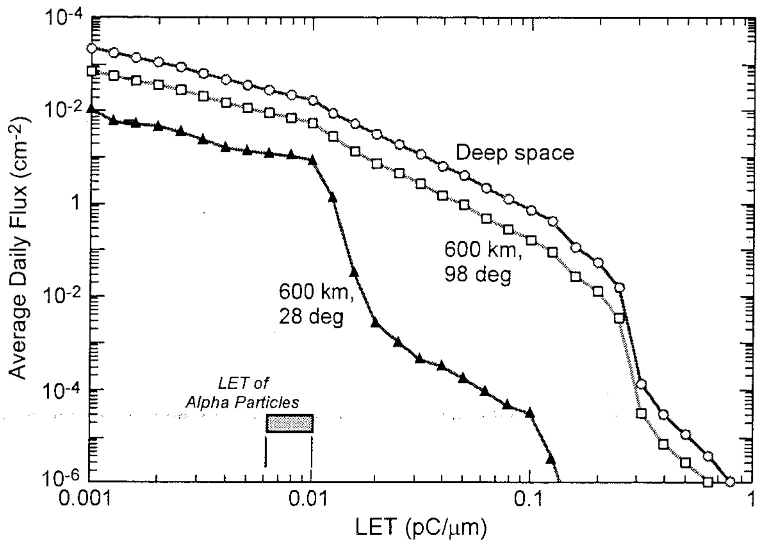
Heavy-Ion Spectrum in Space



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Outline

Single-Event Upset

- Basic issues
- Effects in memories

Solid-State Recorders

- Interactions from heavy ions and protons
- Upset effects in typical flash devices
- Predictions for highly scaled devices

Output Transients in Linear Circuits

Latchup

- Catastrophic damage
- Current detection and shutdown

Conclusions

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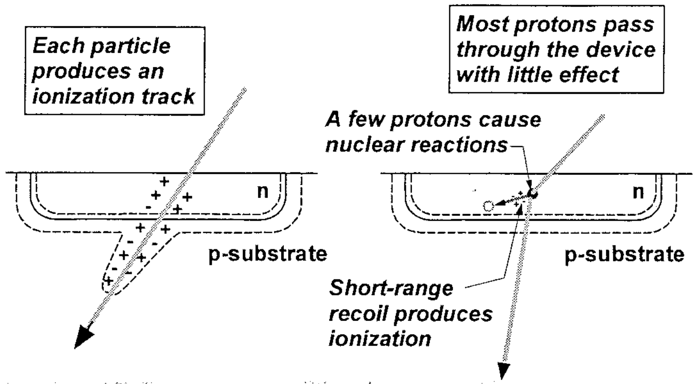
Single-Event Upset



a) Heavy Ions *(ionization by each particle)*

b) Protons *(nuclear reaction needed to produce recoil)*

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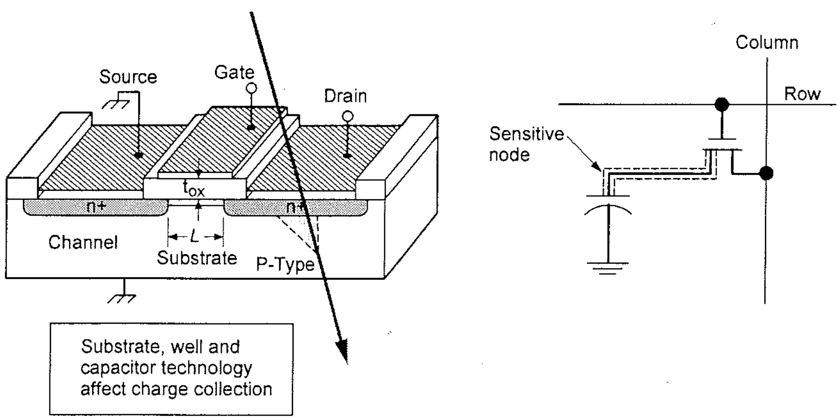
Single-Event Upset in DRAMs



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SEE Upset in Practice

More Complex Failure Modes Can Occur

- SER can place device into test mode without external command
- Other operational modes may also be affected by SEU

Mulitple-Bit Upset Is a Major Concern

Latchup May also Occur

- Not a factor for older DRAMs
- Catastrophic latchup observed for many types of 256-Mb DRAMs

DRAMs Are Extremely Sensitive to SEU

- Protons with energies > 10 MeV
- Alpha particle limit used as baseline for design (~0.01 pC/μm)
- Heavy ions in space with LET > 0.01 pC/μm

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Flash Memories

Attractive Alternatives to DRAMs

Storage cells are relatively immune to upset

Flash Memories Are Extremely Complex

- Internal state machine
- Storage buffers
- Very limited status information
- Causes very complex failure modes

Total Dose Degradation of Charge Pump Limits Space Applications

- Can be mitigated operationally by selectively powering devices during operation
  - Total dose degradation much lower for unbiased conditions
  - Most space applications have limited time windows for data access
- Total dose degradation not a factor in terrestrial applications

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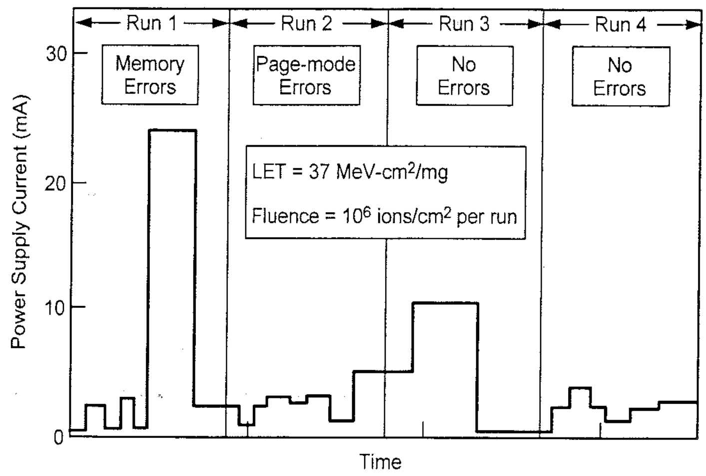
Results of a Sequence of Accelerator Runs on Performance of a 64-Mb NAND Flash Memory



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Solid State Recorder Used on Clementine

(short duration mission to map the Earth's moon)

Designed with Hitachi 4-Mb DRAMs

- Total memory size 2.1 Gbits
- EDAC used for error mitigation
- Corrected errors logged during mission

Recorder Placed in Shielded Case to Reduce Proton Fluence

Performance in Space

- Recorder worked perfectly during a six-month period in space
- Error rate was nearly constant (71 errors per day)
- Predicted error rate was 94 errors per day based on ground test data for DRAMs
- EDAC was effective - 1.5 million images were collected with no errors

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Solid State Recorder Used on Cassini
(long duration mission to explore Saturn)

Designed with OKI 4-Mbit DRAMs
- 640 DRAMs and 18 ASICs
- 2.5 Gbits of memory

Error Correction
- 39-bit word length (32 bits for data, 7 bits for EDAC)
- Detects and corrects single-bit errors; double-bit detection (uncorrected)

Error Rates
- ~ 280 single-bit errors per day, close to predicted values
- EDAC algorithm predicts one uncorrected error every 100 years, but a significant number of uncorrected errors was observed during flight!
- Caused by use of multiple bits within the same memory chip
  - Basic design oversight
  - Architecture considered address space, but not the physical layout

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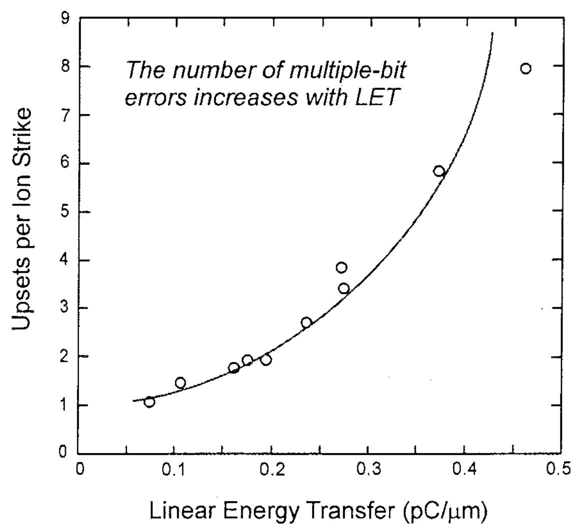
Accelerator Test Results for Multiple-Bit Errors

Multiple-bit error probability increases at high LET

Data shows mean number of upsets, but up to 60 upsets can be observed for some events



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Solid-State Recorder Perspective

EDAC Is Effective in Error Mitigation for Older DRAM Technology

- Multiple bit errors and undocumented test modes must be taken into account
- Recorder architecture must consider physical location of multiple errors, not just address space

Newer DRAMs Are Far More Complex

- Makes error correction more difficult
- Solved by thorough radiation testing and evaluation

DRAM Radiation Sensitivity Has Actually Improved with Scaling

- Primarily due to more compact capacitor structures
- Also influenced by cell size
  - Smaller fraction of deposited charge is collected
  - Particularly important for long-range ions that deposit charge deep within the substrate

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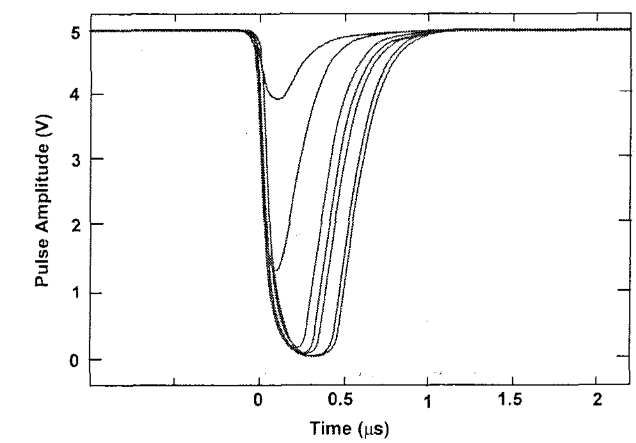
Comparator Upsets from High-Energy Protons

Amplitude depends on location of ion strike

Many pulses have sufficient amplitude to cause errors in digital logic

Error rate depends on differential input voltage, but errors still occur even for high input overdrive



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Mitigation Methods for Soft Errors and Related Radiation Effects in Spacecraft

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The research in this presentation was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration, under the NASA Parts and Packaging Program, Code AE

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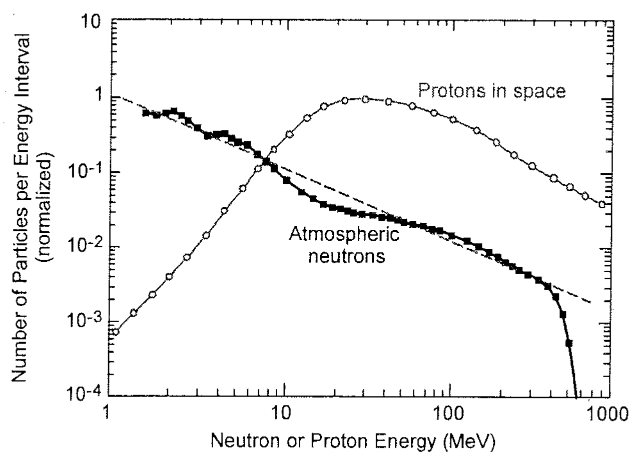
Introduction

- There are many similarities between soft errors from terrestrial and space radiation
- Event rates are higher in space
- Proton flux decreases at low energies, but terrestrial neutron flux increases



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Upsets in Cassini Power Switch

Approximately 10 Upsets per Year Occurred in Power Switch Modules

- Deep space environment
- Special hybrid devices with many components
- Switches were inadvertently triggered into standby mode

Problem Traced to Transient in Basic Comparator (LM139)

- Caused by heavy ions in space
- Designers overlooked possibility of transients in linear devices

Corrected "After the Fact" by Changing Operational Conditions

- Relatively low error rate
- Power switches operational commands reissued approximately once per week

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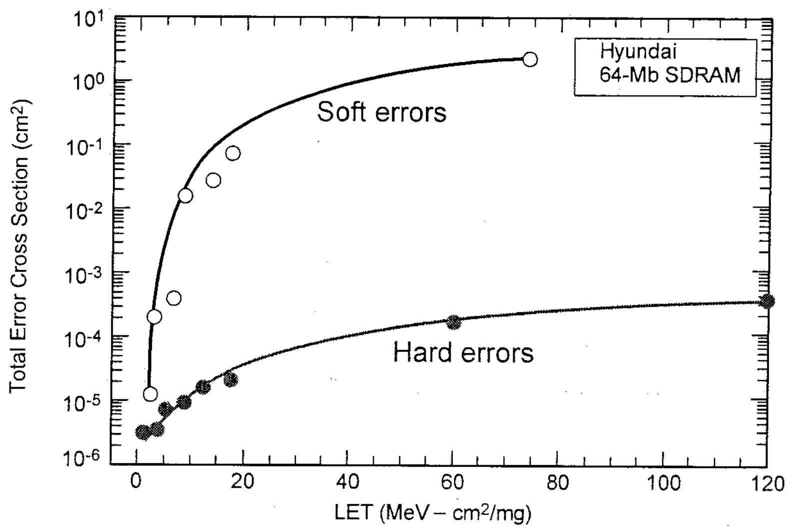
Hard Errors in Advanced DRAMs



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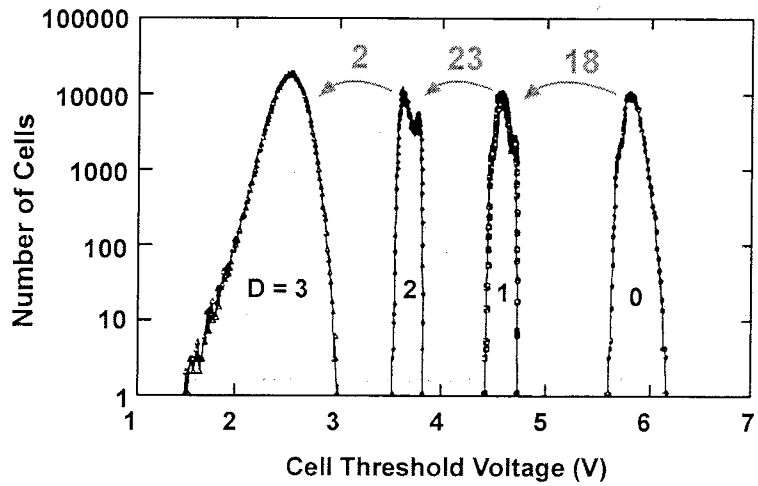
JPL Storage Cell Shift in Multi-Flash Memory Cells from Heavy Ions



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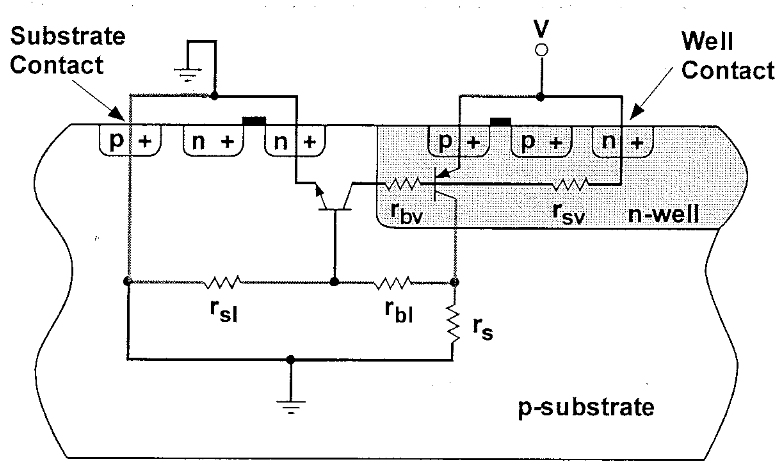
JPL **Single-Particle Latchup**



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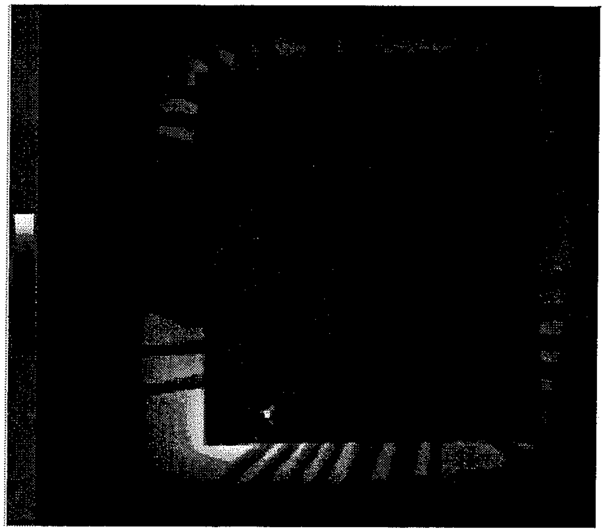
Thermal Image of Localized Heating During Latchup

Extreme localized heating occurs during latchup

Failure can be caused by heating of semiconductor regions, or melting of metallization



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Metallization Damage from Latchup
(200 mA for 0.1 seconds)

High current density causes localized melting

Latent damage is possible from voids created by ejected metal

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Latchup Mitigation

Current Increase Can Be Detected, Triggering Power Shutdown Sequences

Difficult to Do Effectively

- Hundreds of latchup sites are present in modern circuits
- Current surge and damage threshold vary for different sites
- Power system on circuit boards are complex
  - Shutdown times are longer than for laboratory power supplies
  - Large capacitors permit high surge currents
  - Input and output may be overstressed unless they are disconnected

Latchup Mitigation Is a Solution of Last Resort

- Very expensive evaluation tests are required
- Latent damage from latchup may affect reliability

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Conclusions

SER Mitigation Methods Are Routinely Used in Space Systems

- DRAM-based solid-state recorders are baselined for many systems
- Older solid-state recorders have performed well in space
- Complexity of modern DRAMs presents new challenges for mitigation

Mitigation Methods for Microprocessors Have Not Been Developed

- Most space systems rely on special hardened processors
- Processor responses are very complex: crashes and hangs

Space Environment Is More Stringent that Atmospheric Environment

- Much higher event rate
- Increases importance of latchup and multiple-bit upset (as well as transients)

Device Scaling Less Important than Complexity and Architecture

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